

1. A method of forming an antifuse based interconnect structure having amorphous Si antifuse with SiN sidewalls spacers, comprising the steps of:
 - a) providing active elements in a semiconductor substrate;
 - b) forming a first interconnect structure, contacting said active elements, in said semiconductor substrate;
 - c) depositing an insulator layer, on said first interconnect structure;
 - d) forming a via hole in said insulator layer, exposing top surface of said first interconnect structure;
 - e) forming a metal plug in said via hole;
 - f) forming an antifuse, contacting said metal plug; said antifuse comprised of amorphous silicon;
 - g) forming antifuse spacers on the sidewalls of said antifuse; said antifuse spacers are composed of silicon nitride;
 - h) forming a metal layer over said antifuse spacers and said antifuse; and
 - i) patterning by etching said metal layer to form a second interconnect structure, contacting said antifuse layer whereby said antifuse spacers protect said anti-fuse from the etching of said metal layer.

2. The method of claim 1 wherein the step (i) of patterning by etching said metal layer to form a second interconnect structure, comprising:
 - (2a) forming a photoresist pattern over said metal layer;
 - (2b) etching said metal layer to form a second interconnect structure, contacting said antifuse; the etching comprises a RIE process using Cl_2 or BCl_3 etchants; whereby said antifuse spacers protect said antifuse from said etchants and said antifuse spacers are used as an endpoint detection; and whereby the etching creates a polymer on the antifuse spacers'
 - (2c) removing said photoresist layer using a stripper; and
 - (2d) removing said polymer using a wet etch where by said antifuse spacer protects said antifuse.

3. The method of claim 1 wherein said antifuse spacers have a thickness of between about 100 and 2000 Å.
4. The method of claim 1, wherein said active elements in said semiconductor substrate, are MOSFET devices, configured in a gate array pattern.
5. The method of claim 1, wherein said first interconnect structure is formed from an underlying aluminum based layer, containing between about 0 to 3% copper, and between about 0 to 1% silicon, at a thickness between about 1000 to 10,000 Angstroms, and an overlying titanium nitride layer, at a thickness between about 1200 to 1600 Angstroms.
6. The method of claim 1, wherein said first interconnect structure can be formed from a material selected from the group of tungsten, titanium-tungsten, or tungsten silicide.
7. The method of claim 1, wherein said insulator layer is silicon oxide, deposited using PECVD procedures, and planarized using CMP procedures, to create a final thickness, for said insulator layer, between about 0.8 to 3 μm.
8. The method of claim 1, wherein said via hole, in said insulator layer, is formed via anisotropic RIE, using CHF₃ as an etchant, with said via hole having a diameter between about 0.4 to 1.5 μm.
9. The method of claim 1, wherein said metal plug, in said via hole, are formed by anisotropic RIE etch back procedures, using either CF₄—O₂, NF₃—O₂, or SF₆—O₂ as an etchant.
10. The method of claim 1, wherein said antifuse layer, is a composite layer, comprised of an amorphous silicon layer, deposited using PECVD procedures, at a temperature between about 350° to 450° C., to a thickness between about 800 to 1200 Angstroms.
11. The method of claim 1, wherein said second interconnect structure is formed from an aluminum based layer, containing copper, silicon, titanium nitride, or titanium-tungsten.

12. A method for forming an antifuse based interconnect structure with a antifuse comprised of amorphous Si and having antifuse spacers on the sidewalls of said antifuse, comprising the steps of:

- a) providing active elements in a semiconductor substrate;
- b) forming a first interconnect structure contacting said active elements, in said semiconductor substrate;
- c) depositing a first insulator layer; said first insulator layer comprised of silicon oxide;
- d) planarizing said first insulator layer;
- e) opening a via hole in said first insulator layer, exposing top surface of said first interconnect structure;
- f) depositing a first titanium nitride layer, coating the sides of said via hole;
- g) depositing a tungsten layer, completely filling said via hole to form a metal plug;
- h) depositing an amorphous silicon layer over said metal plug and said first insulator layer;
- i) patterning of said amorphous silicon layer, to form an antifuse, and
- j) forming antifuse spacers on the sidewalls of said antifuse; said antifuse spacers composed only of silicon nitride; said antifuse spacers are used as an endpoint detection;
- k) forming a metal layer over said antifuse spacers and said antifuse;
- l) forming a photoresist pattern over said metal layer;
- m) etching said metal layer to form a second interconnect structure, contacting said antifuse; the etching comprises a RIE process using Cl_2 or BCl_3 etchants; whereby said antifuse spacers protect said antifuse from said etchants and whereby the etching creates a polymer on the antifuse spacers;
- n) removing said photoresist layer using a stripper;
- o) removing said polymer using a wet etch where by said antifuse spacer protects said antifuse.

13. The method of claim 12 wherein said antifuse spacers have a thickness of between about 100 and 2000 Å.
14. The method of claim 12 wherein said active elements in said semiconductor substrate are MOSFET devices, configured in a gate array pattern.
15. The method of claim 12 wherein said first interconnect structure is formed from an underlying aluminum based layer, containing between about 0 to 3% copper, and between about 0 to 1% silicon, at a thickness between about 3000 to 5000 Angstroms, and an overlying titanium nitride layer, at a thickness between about 1200 to 1600 Angstroms.
16. The method of claim 12 wherein said first insulator layer is silicon oxide, deposited using PECVD procedures, and is planarized to a final a thickness between about 0.8 to 3.0 µm.
17. The method of claim 12 wherein said via hole is formed in said first insulator layer, via anisotropic RIE procedures, using CHF₃ as an etchant.
18. The method of claim 12 wherein said first titanium nitride layer is deposited using r.f. sputtering, to a thickness between about 800 to 1200 Angstroms.
19. The method of claim 12 wherein said tungsten layer is deposited using LPCVD procedures, at a thickness between about 4000 to 6000 Angstroms.
20. The method of claim 12 wherein said titanium nitride spacers, and said tungsten plug, are formed in said via hole, via anisotropic RIE procedures, using Cl₂ as an etchant.
21. The method of claim 12 wherein said amorphous silicon layer is deposited using LPCVD procedures, at a temperature between about 350° to 450° C., to a thickness between about 800 to 1200 Angstroms.
22. The method of claim 12 wherein said antifuse is formed via anisotropic RIE of said amorphous silicon layer, using Cl₂ as an etchant.
23. The method of claim 12 wherein said second interconnect structure is formed from an aluminum based layer, that can contain copper, silicon, titanium nitride, or titanium-tungsten.